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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/073,506	02/11/2002	Robert J. Falster	MEMC 98-1451/2554.1	6190

321 7590 11/29/2002

SENNIGER POWERS LEAVITT AND ROEDEL
ONE METROPOLITAN SQUARE
16TH FLOOR
ST LOUIS, MO 63102

EXAMINER	
ANDERSON, MATTHEW A	
ART UNIT	PAPER NUMBER
1765	

DATE MAILED: 11/29/2002

4

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10/073,506	Applicant(s) FALSTER ET AL.	
	Examiner Matthew A. Anderson	Art Unit 1765	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE ____ MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 February 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *19-40* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *19-40* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *3* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Information Disclosure Statement

1. The information disclosure statement filed 5/23/2002 fails to comply with 37 CFR 1.98(a)(2), which requires a legible copy of each U.S. and foreign patent; each publication or that portion which caused it to be listed; and all other information or that portion which caused it to be listed. It has been placed in the application file, but the information referred to therein has not been considered.

The references listed as made of record in 09/385,108 (i.e. 1-40, 42, 45-61, 64-68, 70-91, 93-110, 112-126, 128-136, and 139-140) are not considered since the 09/385,104 application is not the parent of the present divisional application. See MPEP version August 2001 609 I.2.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 19-34 are rejected under 35 U.S.C. 103(a) as being unpatentable over Park et a. (US 6,045,610) in view of Graef et al. (US 5,935,320).

Park et al. discloses method of manufacturing monocrystalline silicon ingots and wafers. In one aspect of the invention (see abstract) the pull rate of growth is controlled to not cause vacancy or interstitial agglomerates. The wafers thus produced are also free of vacancy and interstitial agglomerates. In col. 2 lines 30-43, point defects such as vacancies or interstitial Si atoms are undesirable for the fabrication of integrated circuit devices using the Si ingot or wafers cut therefrom. Agglomerates are large structures formed from coalescence of point defects. Vacancy agglomerates are also known as COP, LST, FPD. Interstitial agglomerates are also known as L/D agglomerates. (see col. 2 lines 44-62) Control of the V/G ratio where V is the pull rate and G is the temperature gradient of the ingot–melt interface is described in col. 2 lines 62+ and col. 3 lines1-27. Fig. 2 shows that at a critical V/G ratio an ingot will be produced with vacancies at the center and interstitials at the edge when looking as a section of the ingot perpendicular to the pulling axis. In Fig. 4D pure Si ingot is shown which was grown with a controlled critical V/G. The pure Si is described as Si grown without agglomerations of either the vacancy of the interstitial type. (see description starting col. 8 lines 57) As shown in Fig. 4E, the pull rate is modified over the length of the ingot to compensate for thermal gradient changes during the pull from seed to tail. In col. 7 line 66, 8 in. or approximately 200mm wafers are described. Fig. 3D shows that the boundary between the vacancy dominated center region and the interstitial dominated edge region is essentially constant for the constant diameter portion of the ingot. Park et al. incorporates by reference Wolf et al. Vol. 1 chapter 2 which discloses that oxygen associated with agglomerated defects and desirable in the bulk (e.g. at a

certain depth) Si wafer for gettering purposes. (See pages 49 and 59 especially) The diffusion link to annealing defects is given on page 49.

Park et al. does not explicitly disclose annealing the wafers cut from the ingot.

Graef et al. discloses a process for the formation of Si wafers with low defect density. The wafers are formed by controlling the thermal history of the wafer during pulling. The ingot is then cut into wafers. The wafers are annealed at a temperature of at least 1000'C for a time of at least one hour. The wafers formed by Graef et al. have many more small (i.e. point) defects than large (i.e. agglomerated) defects. (see col. 2 lines 50 +) The anneal is then unusually effective in removing the small defects from the Si wafers. In col. 3 lines 10-15 states that the annealed wafers have small defect densities. The anneal is described in col. 4 lines 28-36 as at at least 1000'C and more preferably 1100'C to 1200'C for more than one hour. The atmosphere in the anneal is described as a noble gas such as argon or hydrogen among others. Process parameters of import during annealing are given (col. 1 lines 65+) as time, temperature, atmosphere and the rate of change of the temperature. Longer anneals at higher temperature lower defect densities the most. Longer times at higher temperatures also increase costs. COP's are shown in Fig. 2 to be dissolved by annealing.

It would have been obvious to one of ordinary skill in the art at the time of the present invention to combine the Park et al. agglomerate free wafer with the anneal of very low agglomerate density wafer of Graef et al. because this would have produced a wafer with low densities of both agglomerated and point defects. Motivation is given in

Park et al. which says the removal of defects (both agglomerates and points) is desirable for making integrated circuits on Si wafers.

It would have been obvious to one of ordinary skill in the art at the time of the present invention to anneal at a temperature above 1000'C including from 1100'C-1200'C for more than 1 hour in argon or hydrogen a 200 mm (i.e. one of at least 150 mm) wafer formed with a controlled V/G ratio and having a central axis with interstitials dominated region at the edge and a vacancy dominated region at the center axis where agglomerated vacancy defects are dissolved because Park et al. discloses such a low density agglomerated Si wafer with such distributions of defects, and Graef et al. discloses such an anneal on large (i.e. agglomerated) COP (vacancy) defects in Fig 2.

It would have been obvious to one of ordinary skill in the art at the time of the present invention that the anneal would affect the outer layer of the wafer first since annealing is a diffusion process and the atmosphere (seen at the surface) is a critical process parameter of annealing.

In respect to claim 23-24, it would have been obvious to one of ordinary skill in the art at the time of the present invention to optimize the temperature and time of annealing because both were result effective process parameters given by Graef et al.

In respect to claims 25-28, 39, it would have been obvious to one of ordinary skill in the art at the time of the present invention to optimize the depth of annealing since Park et al. discloses that defects are not desirable near integrated circuit devices which are grown on the wafer surface yet bulk oxide which form at the agglomerations are

beneficial for gettering purposes (see Wolf et al.) and such optimization would have been achieved by only routine experimentation.

In respect to claims 29-32, 40, it would have been obvious to one of ordinary skill in the art at the time of the present invention to optimize the radial extent of the interstitial dominated region to the vacancy dominated region because such is suggested in col. 5 lines 62+ and col. 6 lines 1-15 and such optimization would have been achieved with only routine experimentation.

In respect to claim 35, it would have been obvious to one of ordinary skill in the art at the time of the present invention that the V/G control during growth of the constant diameter portion from solidification to about 1325'C because the G was defined as the temperature gradient at the ingot melt interface and the melting point of Si is about 1420'C and Si cools as it is pulled upward from that interface.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Matthew A. Anderson whose telephone number is (703) 308-0086. The examiner can normally be reached on M-Th, 6:30-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Benjamin Utech can be reached on (703) 308-3836. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 872-9310 for regular communications and (703) 872-9311 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0661.

MAA
November 20, 2002

BENJAMIN L. UTECH
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 1700